28.6 A 1/2.7 inch Low-Noise CMOS Image Sensor for Full HD Camcorders

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Full high-definition (HD) camcorders require over 1920×1080 pixels and 60fps operation in the progressive scanning mode, which approximately corresponds to a 200MHz pixel readout rate. CMOS image sensors are suitable for high-speed image capture and low power consumption. Using these advantages, a progressive 2/3 inch 1920×1080 CMOS image sensor has been reported [1]. A 2/3 inch optical system is still used in professional HD camcorders to obtain the highest image quality. However, consumer HD camcorders need 1/3 inch or 1/2.7 inch optical systems to keep the size small. Furthermore, the trend in modern consumer HD camcorders is to keep increasing the SNR and resolution until they are as high as digital still cameras. Therefore, small pixels with high SNR are indispensable for HD image sensors. Figure 28.6.1 shows the dark current and random noise trends for high-speed CMOS image sensors. Random noise of $4.8e^-_{rms}$ [2] and dark current of 15e⁻/s at 60°C [3] were reported in 2006. In this work, random noise of $3.5e^-_{rms}$ and a dark current of 12.2e⁻/s are achieved by a new CMOS image sensor.

We describe a progressive 1/2.7 inch 1994×1484 CMOS image sensor with double noise canceller and high-gain column amplifier. The image sensor is fabricated using a 0.18μm 1P3M CMOS process with specialized add-on steps for a high SNR photodiode. To realize very low dark current, we have developed customized shallow trench isolation (STI). 2.75×2.75μm² pixels of high saturation and high conversion gain are achieved by using a 2-shared pixel architecture. Sensitivity is increased by a low optical stack, high-refractive index inner microlens [4] and gap-less top microlens. To suppress the readout noise, this CMOS image sensor has low-noise high-gain column amplifiers [5].

Figure 28.6.2 shows the block diagram of the CMOS image sensor. The image sensor runs 60fps in the 2.12Mpixel HD mode with a 48MHz clock input. To eliminate the difficulty of handling analog signals with such a wide bandwidth, a multi-channel readout scheme is used. Four-channel readout with a total BW of 192MHz is realized without increasing the noise component. This image sensor also has a 2.82Mpixel still capture mode. In this mode, the frame rate is lowered to 30fps.

A 4-shared-pixel architecture is widely used to realize small pixels [6, 7]. However, pixel sharing increases sense node capacitance, as floating diffusion (FD) regions are linked in series and interconnect capacitance is added. The increase of FD capacitance causes a degradation in the conversion gain, resulting in more severe requirements on circuit noise. Our 2.75μm pixel, 2-shared pixel architecture is a solution to realize both high saturation and high conversion gain.

Figure 28.6.3 shows the pixel and double CDS architecture. The pixel consists of buried photodiodes (PD1, PD2), transfer gates (M1, M2) for complete charge transfer to FD, a reset MOS transistor (M3) for resetting FD and a source-follower amplifier (M4) for charge-voltage conversion. In this pixel, the select transistor is removed to maximize the fill factor. A saturation of 14000e⁻ and a conversion gain of 75μV/e⁻ are achieved by this 2-transistor/pixel architecture.

The sensor architecture adopted has a switched-capacitor amplifier (first noise canceller), second noise canceller and an output amplifier. The column amplifier consists of a CMOS operational amplifier, an input capacitor (C_0), a feedback capacitor (C_{FB}) and a switch MOS transistor. The amplifier gain is set by the ratio of C_0 to C_{FB}. Gain settings of ×4 and ×16 are employed. The reset level of the pixel is first sampled on C_0. Before the transfer gate of the pixel turns on, the switch MOS transistor controlled by ΦCL is turned off to disconnect C_0 from the column amplifier output so that the sensor reset level is held on C_0. The reset noise of the FD and the dark signal non-uniformity (DSNU) of the pixel are suppressed by this noise clamp operation. Therefore,a low-noise voltage amplified signal is output from the column amplifier to the second noise canceller.

The use of high-gain column amplifiers causes FPN due to variations in the offsets and gains. The CMOS operational amplifier uses a telescopic cascode topology in order to realize high open-loop gain with small layout pitch. However, the telescopic amplifier requires a higher supply voltage. To obtain wide linear range, the amplifier consists of NMOS transistors with low threshold voltages. The column amplifiers attain a high open-loop gain of 70dB and sufficient linear range of $2.2V_{p\text{-}p}$. Symmetric capacitor layout is also necessary to reduce gain variations in the column amplifiers. The measured non-uniformity in the column gains is 0.08%. The DSNU of vertical stripes caused by the column amplifiers are removed by the second noise cancellers. The individual noise canceller consists of line memories (C_{TN} and C_{TS}) and each line memory stores the reset level of the column amplifier (N) and photo signal level ($N + S$) individually. Thus, the DSNU is eliminated by subtracting voltages stored on C_{TN} from the voltage on C_{TS}.

Figure 28.6.4 is the cross-sectional view of the pixel with on-chip color filter and microlens. The third metal layer is not necessary for effective pixels, but is used as a light-shielding layer of optical black pixels. The thicknesses of metal layers and insulation layers are reduced compared with a conventional CMOS process. The shapes of both top and inner microlenses fabricated at the top of the pixel structure are controlled to gather rays of incident light around the photodiodes. The lens gaps between the microlenses are reduced to improve light gathering efficiency. To realize a large fill factor and small dark current, we have developed a new STI process. A conventional STI structure and the newly developed STI structure are shown in Figure 28.6.4. The conventional STI structure does not have a low dark current because of stress in the STI. By modifying the STI process and the following thermal process, and optimizing the impurity density profile of the channel stop region, very low dark current is attained.

Specifications and characteristics are summarized in Figure 28.6.5. The measurements are performed with the sensor running at 60fps. A 4-channel output architecture realizes a 192MHz data rate with a master clock of 48MHz. The measured power consumption is 220mW. The image sensor has RMS random noise of 4.6e⁻ with a saturation level of 14000e-, the resulting DR is 69.6dB. This random noise is reduced to 3.5e⁻ with G = 16. A low dark current of 0.7e⁻/s at 27°C and a high sensitivity of 14600e⁻/lx·s are achieved by the new pixel structure. Figure 28.6.6 is a reproduced image with 2.12Mpixels taken by the CMOS image sensor. Figure 28.6.7 shows a chip micrograph.

Acknowledgments:
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References:
[1] L. Kozlowski et al., "Progressive 1920×1080 Imaging System on- Chip for HDTV Cameras," *ISSCC Dig. Tech. Papers*, pp.358-359, Feb., 2005.
[2] Y. Nitta et al., "High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor," *ISSCC Dig. Tech. Papers,* pp. 500-501, Feb., 2006.
[3] S. Yoshihara et al., "A 1/1.8-inch 6.4Mpixel 60 Frames/s CMOS Image Sensor with Seamless Mode Change," *ISSCC Dig. Tech. Papers,* pp. 492-493, Feb., 2006.
[4] T. Yamada et al., "Improvement of Photo-Sensitivity and Smear Characteristics in 2.8-μm Square Pixel IT-CCD Image Sensor," *IEEE Workshop on CCDs and Advanced Image Sensors,* 2003.
[5] S. Kawahito et al., "A Column-Based Pixel-Gain-Adaptive CMOS Image Sensor for Low-Light-Level Imaging," *ISSCC Dig. Tech. Papers,* pp. 224-225 Feb., 2003.
[6] H. Takahashi et al., "A 3.9μm Pixel Pitch VGA Format 10b Digital Image Sensor with 1.5-Transistor/Pixel," *ISSCC Dig. Tech. Papers,* pp. 78-79, Feb., 2004.
[7] R. D. McGrath et al., "Shared Pixels for CMOS Image Sensor Arrays," *IEEE Workshop on CCDs and Advanced Image Sensors,* pp. 9-12, 2005.

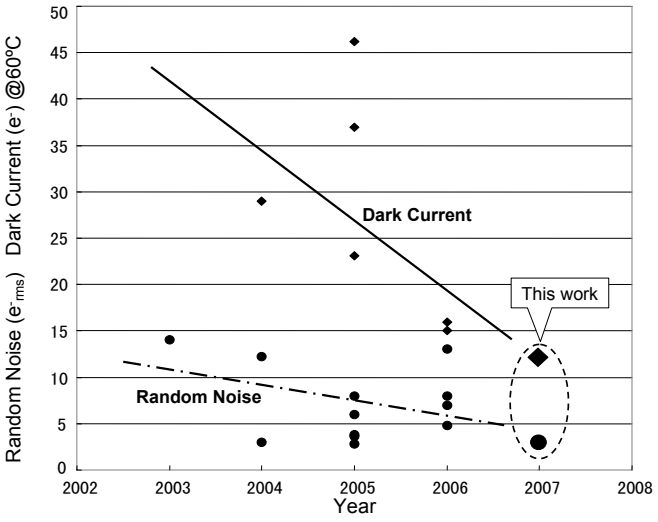

Figure 28.6.1: Random noise and dark current trends for CMOS image sensors.

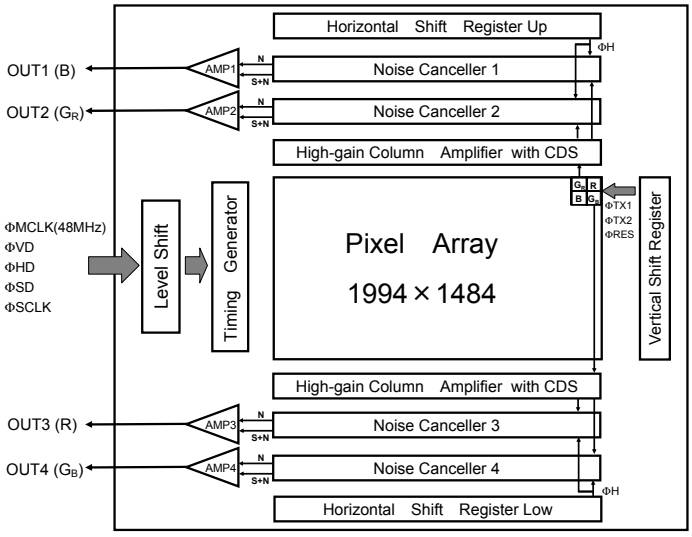

Figure 28.6.2: Block diagram of the CMOS image sensor.

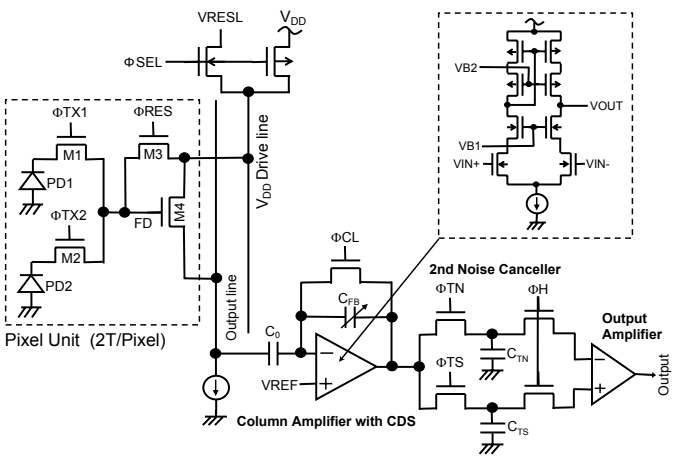

Figure 28.6.3: Pixel and double CDS architecture.

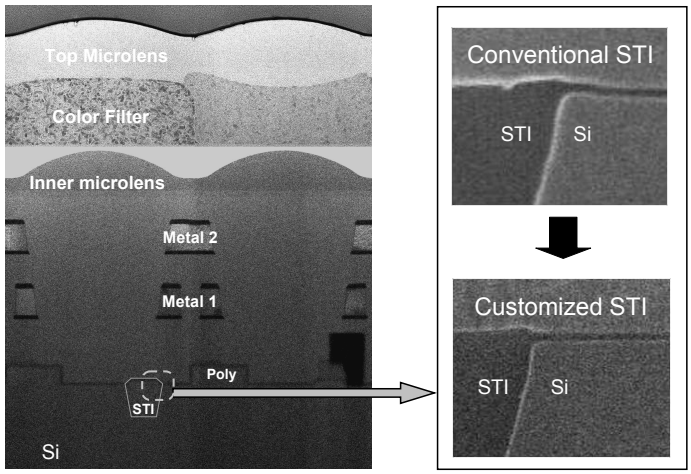

Figure 28.6.4: Cross-sectional view of the pixel.

Process	0.18μm 1P 3M CMOS
Chip size	7.6mm(H)x7.8mm(V)
Pixel size	2.75μm(H)x2.75μm(V)
Number of effective pixels	1944(H)x1452(V)
Pixel rate	192MHz (48MHz × 4ch)
Maximum Frame rate	60frames/s
Column gain stage	×4、×16
Mode	2.12M Full HD movie 2.82M Still capture
Conversion gain	75μV/ e-
Sensitivity (Green pixels)	14600e-/lx s (2856k light source With IR cut filter)
Saturation full well	14000e- (@60℃)
PRNU (Green pixels)	0.58%(@50% saturation)
DSNU (of full well)	0.01%
Dark current	0.7e-/s (@RT) 12.2e-/s (@60℃)
RMS random noise	4.6e- (@column gain = 4) 3.5e- (@column gain = 16)
Dynamic range	69.6dB (@column gain = 4)
Power consumption	220mW (60frames/s)

Figure 28.6.5: Specification and characteristics of the image sensor.

Figure 28.6.6: Reproduced image.

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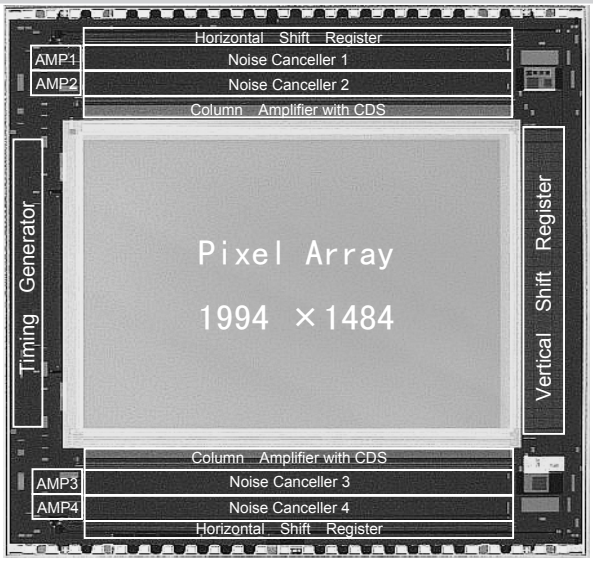

Figure 28.6.7: Chip micrograph.

